Tektronix Logic Analyzers

▶ TLA7N4 Logic Analyzer Module

▶ The TLA Series logic analyzer modules offer the highest performance for today's demanding applications.

Breakthrough Solutions for Real-time Digital Systems Analysis

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7N4 logic analyzer module answers the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture and analyze real-time digital system operation in order to debug, verify, optimize and validate digital systems. Hardware developers, hardware/software integrators and embedded software developers will appreciate the range of capabilities of the TLA7N4 logic analyzer module. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state and high-speed timing analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, non-intrusive software execution tracing that correlates to source code and to hardware events; and non-intrusive probing.

The TLA7N4 logic analyzer module offers Tektronix' breakthrough MagniVu™ technology for providing high-speed sampling (up to 2 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities.

The TLA7N4 module offers high-speed state synchronous capture and high-speed timing capture through the same set of probes. It capitalizes on MagniVu technology to offer 500 ps timing on all channels, glitch and setup/hold triggering and display, and timestamp that is always on at up to 500 ps resolution.

The TLA7000 Series logic analyzer modules are ideal for timing analysis, multi-processor/bus applications and embedded software analysis.

▶ Features & Benefits

136 Channel Logic Analyzer with up to 8 Mb Depth

MagniVu™ Acquisition Technology Provides 2 GHz (500 ps) Timing Resolution to Find Difficult Problems Quickly

Up to 200 MHz State Acquisition Analysis of Synchronous Digital Circuits

Simultaneous State and High-speed Timing Analysis Through the Same Probe Pinpoints Elusive Faults Without Double Probing

500 MHz Deep Timing Analysis with Up to 8 Mb Per Channel

Glitch and Setup/Hold Triggering and Display Finds and Displays Elusive Hardware Problems

Transitional Storage Extends the Signal Analysis Capture Time

Broad Processor and Bus Support

Full Range of General-purpose and High-density Non-intrusive Probes

▶ Applications

Hardware Debug and Verification

Processor/Bus Debug and Verification

Embedded Software Integration, Debug and Verification

Tektronix

Enabling Innovation

▸ Characteristics

General

Number of Channels (all channels are acquired including clocks) –
TLA7N4: 136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping – No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).
Module "Merging" –
Three modules can be "merged" to make up to a 408-Channel module. Merged modules exhibit the same depth as the lesser of the three individual modules. Word/range/setup-and-hold/glitch/transition recognizers span all three modules. Only one set of clock connections is required.
Time Stamp –
50-Bit at 500 ps resolution (6.5 day range).
Clocking/Acquisition Modes –
Internal, internal 2X, external. 2 GHz MagniVu™ high-speed timing is available simultaneous with all modes.
Number of Mainframe Slots Required per TLA Series Module – 2.

Input Characteristics (with P6417, P6418, P6419 or P6434 probes)

Capacitive Loading –
<0.7 pF data and clock (P6419).
1.4 pF typical data; 2 pF typical clock (P6418).
2 pF typical data and clock (P6417 and P6434).
Threshold Selection Range –
From +5.0 V to –2.0 V in 50 mV increments.
Threshold Selection Channel Granularity –
Separate selection for clock (1) and data (16) for each 17-Channel probe connector.
Threshold Accuracy (including probe) –
±100 mV.
Input Voltage Range –
Operating: 6.5 V_{p-p} centered around the programmed threshold.
Non-destructive: ±15 V.
Minimum Input Signal Swing –
250 mV or 25% of signal swing, whichever is greater (P6417, P6418 and P6419).
300 mV or 25% of signal swing (P6434).
Input Signal Minimum Slew Rate –
200 mV/ns typical.

State Acquisition Characteristics (with P6417, P6418, P6419 or P6434 probes)

State Clock Rate –
100 MHz standard, 200 MHz optional.
State Data Rate (half/full channels) –
400/200 Mb/s, typical. Requires 200 MHz state option.
State Memory Depth with Timestamps –
64 Kb, 256 Kb, 1 Mb or 4 Mb per channel.
Setup-and-Hold Time Selection Range –
From 8.5 ns before, to 7.0 ns after clock edge.
Setup-and-Hold Window – 2 ns typical.
Minimum Clock Pulse Width – 2 ns.
Active Clock Edge Separation – 5 ns.
Demux Channel Selection –
Channels can be demultiplexed to other channels through user interface with 8-Channel granularity.

Timing Acquisition Characteristics (with P6417, P6418, P6419 or P6434 probes)

MagniVu Timing – 500 ps.
MagniVu Timing Memory Depth –
2 Kb (2048) per channel.
Deep Timing Resolution (half/full channels) –
2/4 ns to 50 ms.
Deep Timing Resolution with Glitch Storage Enabled – 10 ns to 50 ms.
Deep Timing Memory Depth (half/full channels with timestamps and with or without transitional storage) –
128/64 Kb, 512/256 Kb, 2/1 Mb, 8/4 Mb per channel.
Deep Timing Memory Depth with Glitch Storage Enabled – Half of default main memory depth.
Channel-to-channel Skew – <1 ns typical.
Minimum Recognizable Pulse Width (single channel) – 2 ns.
Minimum Recognizable Glitch Width (single channel) – 2 ns.
Minimum Recognizable Multi-channel Trigger Event – Sample period +2 ns.

Trigger Characteristics

Independent Trigger States – 16.
Maximum Independent If/then Clauses per State – 16.
Maximum Number of Events per If/Then Clause – 8.
Maximum Number of Actions per If/Then Clause – 8.
Maximum Number of Trigger Events –
18 (2 counter/timers plus any 16 other resources).
Number of Word Recognizers – 16.
Number of Range Recognizers – 4.
Number of Transition Recognizers – 1.
Number of Counter/Timers – 2.
Trigger Event Types –
Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation.
Trigger Action Types –
Trigger module, trigger all, store, don't store, start store, stop store, increment counter, reset counter, start timer, stop timer, reset timer, goto state, set/clear signal, do nothing.
Trigger Sequence Rate – DC to 250 MHz (4 ns).

Counter/Timer Range –
51 Bits each (>100 days at 4 ns).
Counter Rate – DC to 250 MHz (4 ns).
Timer Clock Rate – 250 MHz (4 ns).
Counter/Timer Latency –
None (can be tested or reset immediately after starting).
Range Recognizers –
Double bounded (can be as wide as any group, must be grouped according to specified order of significance).
Setup-and-Hold Violation Recognizer Setup Time Range –
From 8 ns before to 7 ns after clock edge in 0.5 ns increments.
Setup-and-Hold Violation Recognizer Hold Time Range –
From 7 ns before to 8 ns after clock edge in 0.5 ns increments.
Trigger Position – Any data sample.
MagniVu™ Trigger Position –
MagniVu data is centered around the module trigger.
Storage Control (data qualification) –
Global (conditional), by state (start/stop), by trigger action or transitional.
Storage Window Granularity –
Single sample or block-of-31 samples before and after.
Safety –
CSA C22.2 No. 1010.1, EN61010-1, IEC61010-1, UL 3111-1.

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net (without probes)	3.1	6.7
Shipping (typical)	6.3	13.7

▸ Ordering Information

TLA7N4 Logic Analyzer Module

Includes: Probe retainer bracket, probe manual, certificate of calibration, one-year warranty (return to Tektronix) and user manual.

Probes must be ordered separately.

TLA7N4 – 136-Channel Logic Analyzer module, 2 GHz timing, 100 MHz state, 64 Kb depth. Options for up to 4 Mb depth and/or 200 MHz state.

Logic Analyzer Module Options

(Base configuration is 64 K depth at 100 MHz state.)

Opt. 1S – Increase to 256 K depth at 100 MHz state.

Opt. 2S – Increase to 1 M depth at 100 MHz state.

Opt. 3S – Increase to 4 M depth at 100 MHz state.

Opt. 4S – Increase to 64 K depth at 200 MHz state.

Opt. 5S – Increase to 256 K depth at 200 MHz state.

Opt. 6S – Increase to 1 M depth at 200 MHz state.

Opt. 7S – Increase to 4 M depth at 200 MHz state.

TLA7N4 Service Manual and Test Fixtures

TLA7N4 Logic Analyzer Performance Verification and Adjustment Fixture (includes AC adapter; requires local power cord – Order 671-3599-00.

TLA7N4 Logic Analyzer Modules Service Manual (includes Performance Verification and Adjustment procedures) – Order 071-0864-01.

TLA Series Module Upgrades

You can increase the memory depth and state speed of most existing TLA Series logic analyzer modules. You can also install a TLA7N4 logic analyzer module into an existing TLA715/721/7XM/7012/7016 mainframe. Please refer to the TLA Family Upgrade Guide for further details.

Logic Analyzer Probe Selection Guidelines

There are a number of flexible choices of logic analyzer probes available for use with TLA Series logic analyzer modules. Please see logic analyzer probe data sheets for more information.

Logic Analyzer Module Probes and Accessories

TLA7N4 Service Options

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report.

Opt. D3 – Calibration Data Report 3 Years (with Opt. C3).

Opt. D5 – Calibration Data Report 5 Years (with Opt. C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

Opt. IN – Product Installation Service.

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Contact Tektronix:

ASEAN / Australasia / Pakistan (65) 6356 3900
Austria +41 52 675 3777
Balkan, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium 07 81 60166
Brazil & South America 55 (11) 3741-8360
Canada 1 (800) 661-5625
Central East Europe, Ukraine and Baltics +41 52 675 3777
Central Europe & Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France & North Africa +33 (0) 1 69 86 81 81
Germany +49 (221) 94 77 400
Hong Kong (852) 2585-6688
India (91) 80-22275577
Italy +39 (02) 25086 1
Japan 81 (3) 6714-3010
Luxembourg +44 (0) 1344 392400
Mexico, Central America & Caribbean 52 (55) 56666-333
Middle East, Asia and North Africa +41 52 675 3777
The Netherlands 090 02 021797
Norway 800 16098
People's Republic of China 86 (10) 6235 1230
Poland +41 52 675 3777
Portugal 80 08 12370
Republic of Korea 82 (2) 528-5299
Russia & CIS 7 095 775 1064
South Africa +27 11 254 8360
Spain (+34) 901 988 054
Sweden 020 08 80371
Switzerland +41 52 675 3777
Taiwan 886 (2) 2722-9622
United Kingdom & Eire +44 (0) 1344 392400
USA 1 (800) 426-2200
USA (Export Sales) 1 (503) 627-1916
For other areas contact Tektronix, Inc. at: 1 (503) 627-7111

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Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

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